TRIGG AND SYNC VIDEO SIGNALS
TS61

TS61 is designed to synchronize a CVBS signal (Color Video Blanking Synchronization). Such a trigger circuit can be constructed with a relatively small number of components, but if the video signal is scrambled or coded requires a more advanced circuit switching. This option works with the signal from the scart socket and is trigged on the 50Hz vertical sync pulse. To avoid trigging on anything other than the vertical sync pulse of the video signal are there some circuits that seems for just that! When we have a pulse that is synchronous have we also acquired full control of this video signal. That is to say a basic requirement before we can begin to manipulate the signals components. This module uses all the logic circuits required for the generation of horizontal sync pulses that also suppress any disturbances in the CVBS signal. It is possible to achieve if one want to use all sub components (unused gates) in the logic circuits to 100% and that is the real truth in this circuit. Although it not contains any signal interference or distortion can you be sure that the synchronization always is perfect.

TS61 will be included as a module in which something should be done with a video signal. For example; a Macrovision Decoder or for correction of a SSAVI signal (Sync Suppression and Active Video Inversion). It is based on default logic, and requires no pre-programmed ICs.

TS61 works with the same principle as an ordinary TV, in order to synchronize a video signal. The difference is that this synchronization device is even more robust against disturbances and errors in the video signal. For example, if the horizontal sync pulses (also known as line sync pulses) are distorted, could one get a positive response from the V-sync in the middle of an image-building. With the "principle" I suggest that the H-sync pulses are generated by a freely oscillating crystal clocked counter which is reset by the V-sync pulse (flywheel). In the future, perhaps someone would like to introduce countermeasures against this type of decoder? In this case is the step not far from to start tamper with the V-sync pulse. If that leadership began to extend or shorten the V-sync are there different wiring options for the V-sync indicator circuits in the TS61 module. There are opportunities to draw on an &-gate and some tracks associated with that gate, or to replace a resistor, etc. completely depends on what kind of countermeasures that have been introduced. If it becomes necessary at the same time and randomly both prolong and shorten the V-sync will even this decoder circuit probably submit for good? If someone chooses to use TS61 as a trigger circuit in a decoder for SSAVI system - the following should be observed: It has occurred that SSAVI-coding also contains an added sinus signal to the CVBS signal at 50Hz. This means that half of the picture is shaped like a sine wave. Since the input stage is clamped, i.e. DC-related locked, you have to draw up the trigger level in TS61 pretty much in order to be able to trig on it (under the assumption that the V-sync is at the top of the sine wave). If so, drops the adjacent video information’s slowly over the preset trig-level and condition no. 1 is thus eliminated. All conditions can be overcome if one adds the pulses of adjacent lines corresponding to the pulses of a V-sync. TS61 is then inoperative.

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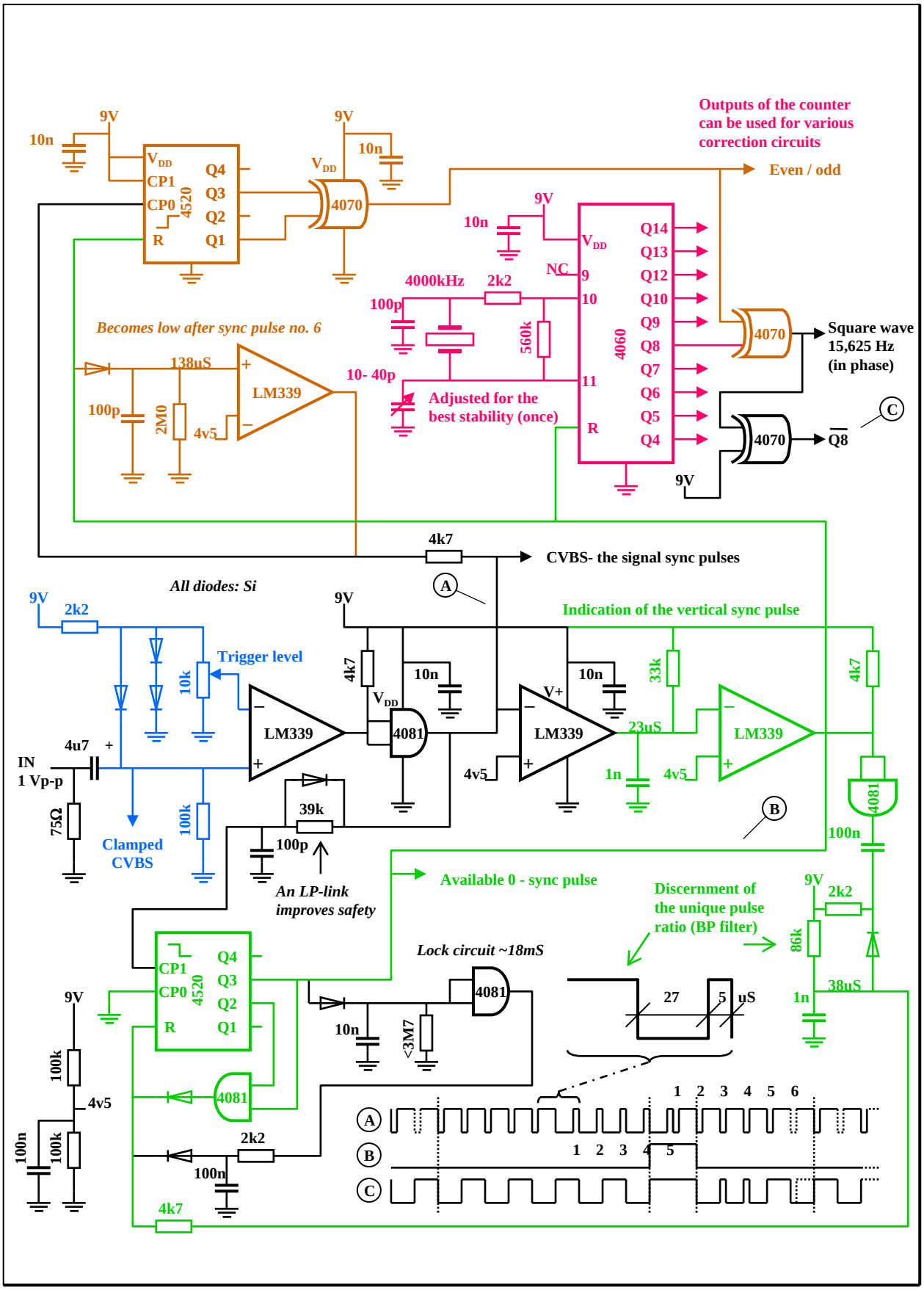
Before TS61 are allowed to operate in such video signal, must the sine wave be removed. The sine wave can be filtered out by a BP-filter. If the filter has duration of half a period can you add it to the video signal again and the sine wave will compensate away itself.

There are five conditions, which must be met in order for a 0-sync pulse shall be generated:
1) A low-level sync (blacker than black level) should be active for in least 23uS.
2) Before 38uS has elapsed since condition 1 was active shall a new low-level sync occur again.
3) The conditions in paragraphs 1 and 2 must be clocked with the inverted countervailing pulse (consistent with a line sync pulse) descending flank, at least 4 times in a row.
4) The inverse countervailing pulse time shall not be less than ~ 3uS before clocking should be done.
5) A temporary disorder that meets all the previous conditions must be located relatively close to the V sync pulse position in the video signal.

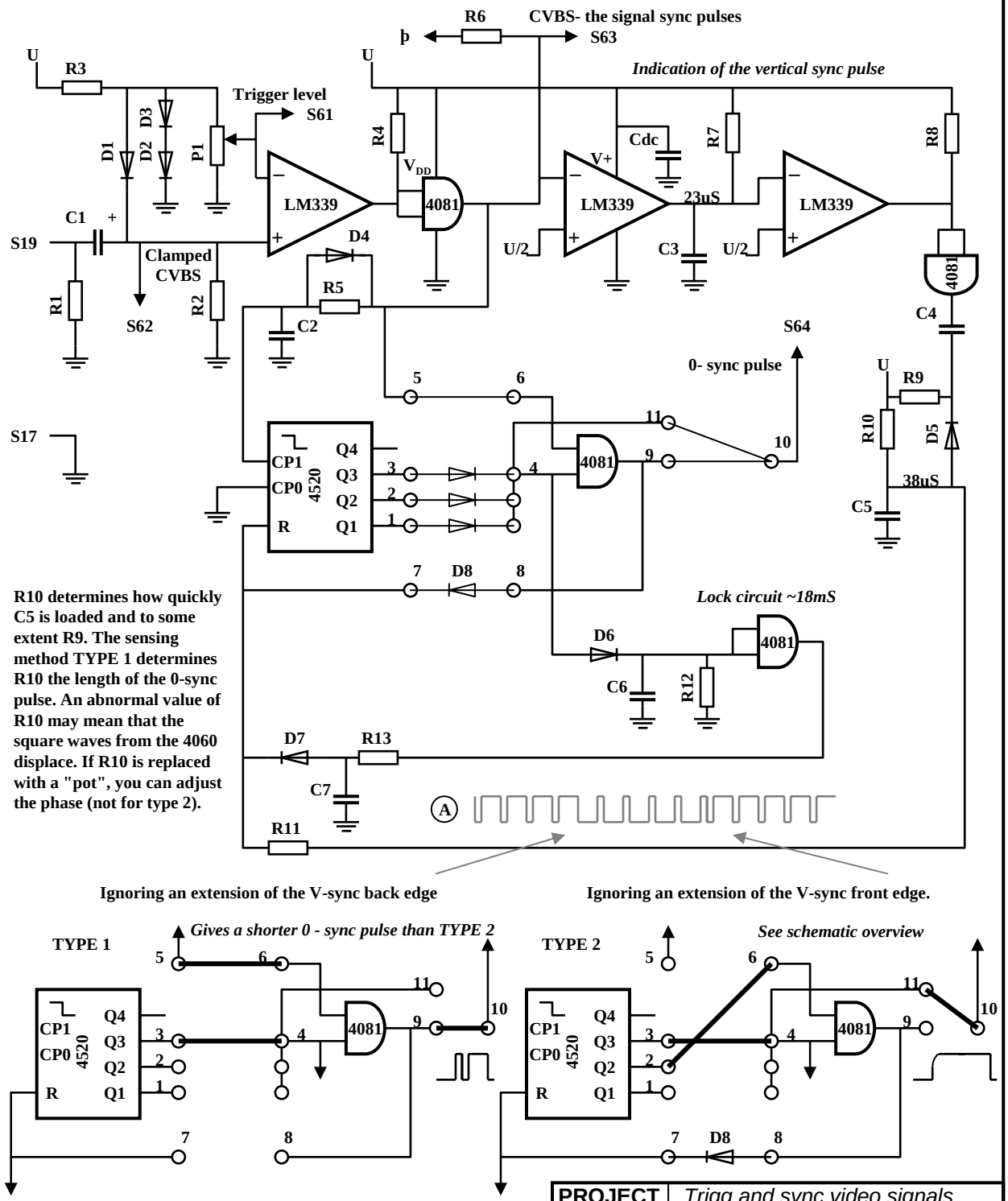
The PCB layout for TS61 is of the type; double-sided printed circuit board and based on SMD technology. It means that the size of the printed circuit board is quite small, even though the design of its execution is directed to the home nick loader. In addition, includes a ground plane which effectively keeps interfering radiation from the device at a low level. The ground plane contains no tracks which will facilitate the construction. Only holes to the ground plane needs to be drilled, which means that you in principle can use a single-sided board and on the other hand, choosing a piece of sheet metal which may serve as a ground plane. If you make the sheet metal piece larger than the board’s dimensions can you bend up the edges and screen the whole caboodle. Connections similar to PNP (PC card), is designed for copper tracks on an “prototyping board". Then there exist the possibility to using a prototyping board as a system bus where TS61 are included in a larger context. TS61 can then be soldering perpendicular to the prototyping board. The same board can then in turn directly be solder on a dismantled scart-connector, or you can e.g. drill holes in the board and screw the module into an appliance box. The board also includes some hole-mounted components. All ICs that are hole-mounted can be regarded as surface-mounted components. A difference that only is imaginary. And if you want to shorten the IC legs (by cut theme), so you can do it too.

The setting of TS61 to a video signal is simple. An indicator circuit is included in the bargain that one not have an oscilloscope for adjust the "trigger level" with P1. Just turn P1 until the green LED lights. If the amber blink is there less V-sync pulses than normal and if the red blinks are there more V-sync pulses than normal. An oscilloscope is necessary when you with C10 must minimize the line sync pulses from phase drift. The clamping circuit for TS61 is the traditional type, and works well in most cases. If we again have to face to one of the video signal that superimposed a sine wave is the method of clamping inadequate but not if the sine wave is stable. If the sine wave varies in amplitude requires a more sophisticated method of clamping. It does not necessarily mean that TS61 not can be used anymore. In that case you can solder away associated diodes and the potentiometer for adjustment of the trigger level. Then you can plug in a circuit that works better. For decoding of Macrovision is TS61 overqualified in terms of performance but it is good to be hedged for the future also.

SCHEMATIC OVERVIEW



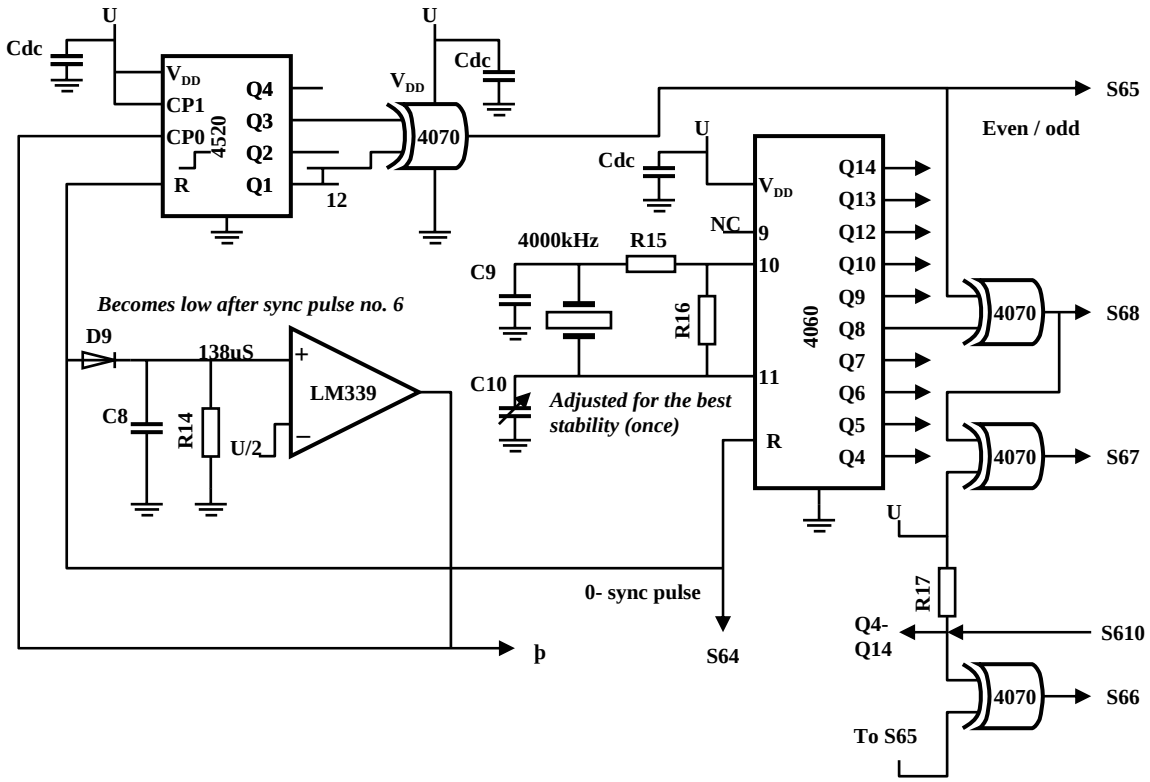
CIRCUIT DIAGRAM



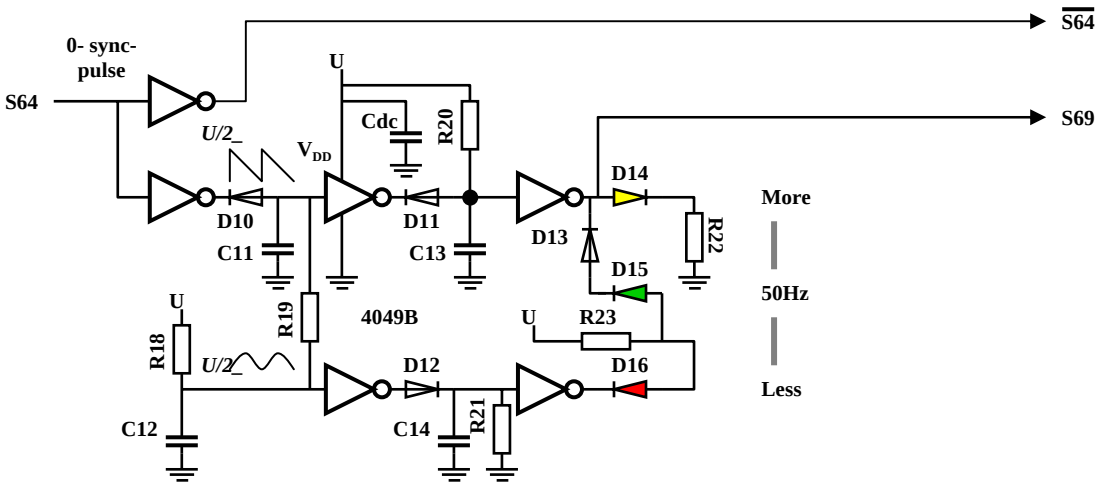
The figure shows two different coupling variants of some of the V-sync indicator circuits. It does not matter which you choose to use. The purpose is to thwart a future scenario in which those responsible has tried to put the decoder inoperative. Diodes that are depicted from Q1-Q3, is to reduce the countdown of the pulse factors on the V-sync pulse. This may be envisaged if the V-sync in the future for any reason will be shortened?

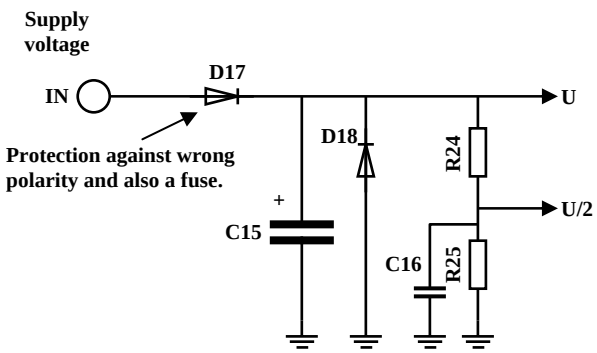
PROJECT	*Trigg and sync video signals*	
MODULE	*Trigg & Synchronize*	
MODEL	**TS61**	**-**
AUDIT	A-1	**DRAWING: 1 of 2**
SUPPLY	≥ +8 VDC	≤ +15 VDC
CURRENT	30 mA	at 12 V
OTHER		
B. Lindqvist		

CIRCUIT DIAGRAM



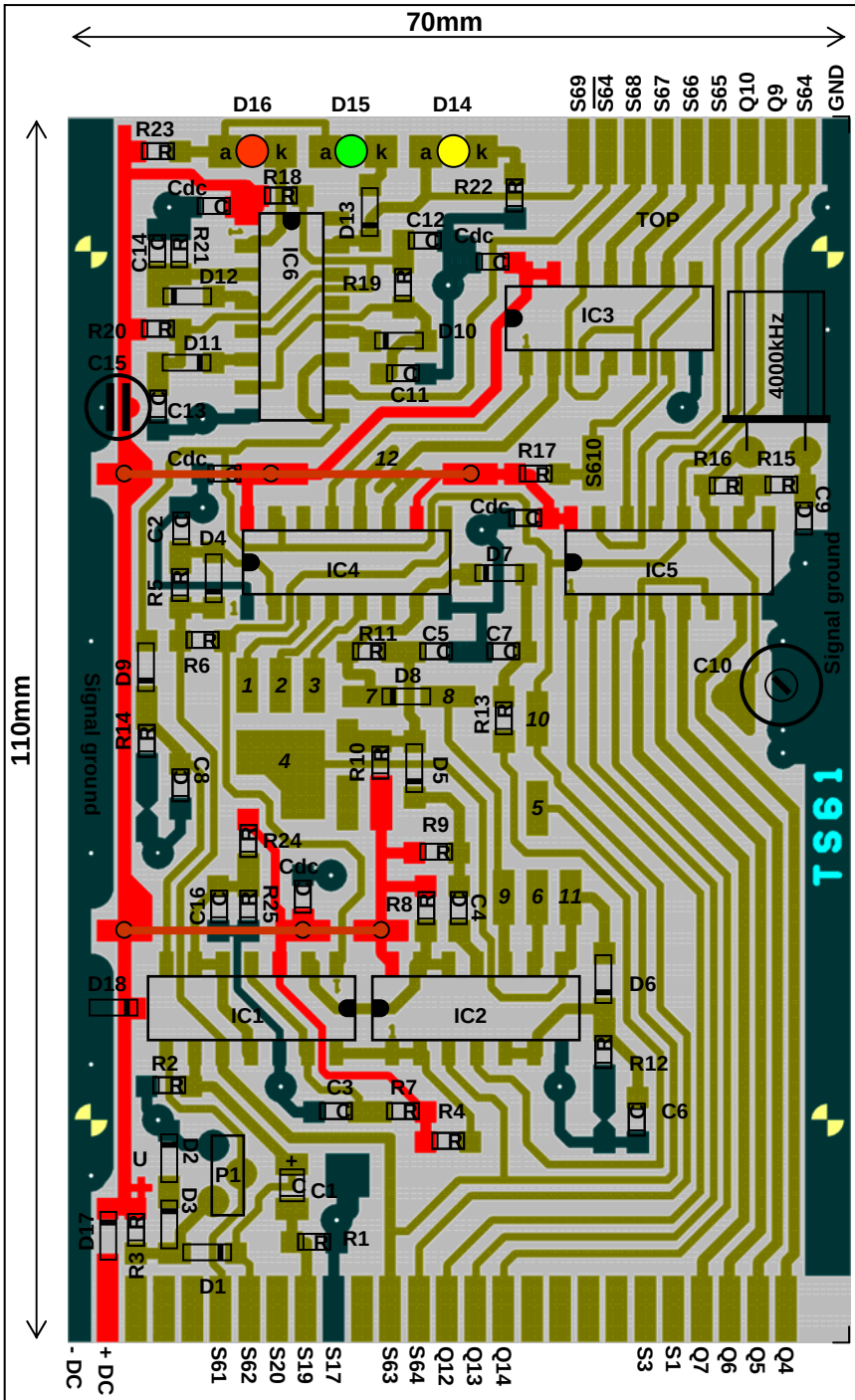
INVERTER AND INDICATOR CIRCUIT FOR THE 0- SYNC PULSE





PROJECT	*Trigg and sync video signals*	
MODULE	*Trigg & Synchronize*	
MODEL	**TS61**	**-**
AUDIT	A-1	**DRAWING: 2 of 2**
SUPPLY	≥ +8 VDC	≤ +15 VDC
CURRENT	30 mA	at 12 V
OTHER		
B. Lindqvist		

PLACING OF COMPONENTS



SMR1206:
R1 = 75Ω
R2 = 100k
R3 = 2k2
R4 = 4k7
R5 = 39k
R6 = 4k7
R7 = 33k
R8 = 4k7
R9 = 2k2
R11 = 4k7
R12 = 3M3
R13 = 2k2
R14 = 2M0
R15 = 2k2
R16 = 560k
R17 = 100k
R19 = 150k
R20 = 2M
R21 = 2M
R24 = 100k
R25 = 100k

SMC1206:
C2 = 100p
C3 = 1n
C4 = 100n
C5 = 1n
C6 = 10n
C7 = 100n
C8 = 100p
C9 = 100p
C11 = 100n
C12 = 100n
C13 = 100n
C14 = 100n
C16 = 100n
Cdc = 10nx5

Other capacitors:
C1 = 4µ7, Tantalum, SMD
C10 = 10-40p, trim. PCB
C15 = 47µ, E-lytic, PCB

IC (hole mounted):
1) LM339, 4x comparator
2) 4081B, 4x &-gate
3) 4070B, 4x exor
4) 4520B, 2x binary counter
5) 4060B, binary counter
6) 4049B, 6x inverter

Other components:
R10 = 82k when U ≥ 10V
R10 = 86k when U < 10V
R18 = 180/U+295 [kΩ]
R22&R23 = $(U-2)/I_{LED}$
D1-D13 = BAS32, SMD
D17&D18 = LL5817, SMD
D14-D16 = LED, 20mA
P1 = 10k trim pot. Standing
One CPU crystal 4MHz

Single side or double sided board. On the ground plane shall 22 ground passages be drilled at the markings on the board. The ground plane can also consist of sheet metal. No other holes need to be drilled, except for the screw holes. For C10 shall two of the legs act as ground passages and also the negative pin on C15. Other comp. is surface mount.

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OTHER	-	
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